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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,852	04/14/2004	Mike Jadon	01SH-109195	6873
30764 7590 01/11/2007 SHEPPARD, MULLIN, RICHTER & HAMPTON LLP 333 SOUTH HOPE STREET 48TH FLOOR LOS ANGELES, CA 90071-1448			EXAMINER BONZO, BRYCE P	
			ART UNIT 2113	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE			MAIL DATE	DELIVERY MODE
3 MONTHS			01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/824,852

Applicant(s)

JADON ET AL.

Examiner

Bryce P. Bonzo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8-17 is/are rejected.
- 7) ☒ Claim(s) 6 and 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Non-Final Official Action

Status of the Claims

Claim 14 is rejected under 35 USC §112, second paragraph.

Claims 1 and 5 are rejected under 35 USC §102.

Claims 2-4, 8-13, 16 and 17 are rejected under 35 USC §103.

Claims 6 and 7 are objected to while containing allowable subject matter.

Multiple Dependency

Claim 15 is unexamined as it is a multiple dependent claim depending from a multiple dependent claim.

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 14, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Reeves (United States Patent No. 7,028,154 B2).

As per claim 1, Reeves discloses:

1. An NVRAM fail-over controller comprising:

An NVRAM device connected to a host computer, the host computer having the ability to directly control the NVRAM device (column 6, lines 4-21);

An embedded processor on the NVRAM fail-over controller that is powered by back-up power (column 6, lines 33-47);

A network interface on the NVRAM fail-over controller that is powered by back-up power (column 5, lines 34-56 and column 6, lines 48-63).

As per claim 5, Reeves discloses:

A controller of claim 1 using non-transparent bus bridges (column lines 44-60: Reeves clearly discloses the use of any bus, including those with non-transparent bridges).

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-13, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reeves (United States Patent No. 7,028,154 B2).

As per claim 8, Reeves does not explicitly disclose:

the ability to add daughter cards.

Official notice is given that it is notoriously well known to provide computer systems with the ability have add-in cards for future upgrades. This is often done for one of two reasons. First, the device is a base model which allows for the addition of memory or other devices and thus may reduce cost. Additionally, this often done in order to allow for upgrades for technology which a manufacturer does not have access to at the time of manufacture. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to implement the well known practice of providing daughter cards in the system of Reeves, thus allowing for extensibility in later usage.

As per claim 9, Reeves discloses:

a network controller under control of the host computer (column 3, lines 58 through column 4, line 14).

As per claim 10, Reeves discloses:

a disk or RAID controller under control of the host computer (column 4, lines 51-65; column 9, lines 45-48).

As per claim 11, Reeves discloses:

a disk or RAID controller under control of the embedded processor (column 6, lines 22-30).

As per claim 12, Reeves discloses:

a RAID device with NVAM under control of the host computer (column 6, lines 22-30; column 9, lines 45-48).

As per claim 13, Reeves discloses:

NRAM device that preserves data during long outages by sending it to another computer over a network or to a disk attached as in claims 10 or 11 and that retrieves such data aback into NVRAM at a later time (column 6, lines 4-63).

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As per claim 16, Reeves does not explicitly disclose:

a watch dog timer to reset the embedded processor.

Official Notice is given that it is notoriously well known to incorporate watchdog timers into controller with embedded processors. Watch dog processors often provide a system with a mechanism to reset in the case of time out. These time outs often occur when the processors hang do to a variety of problems from poorly written code to radiation or memory overflows. The resetting caused by many watch dog timers is used to restart the processor in a known state so that it may continue to operate normally. This greatly increases the fault handling abilities of devices in which watch dog timers are implemented. This it would have been obvious to one of skill in the art at the time of invention to incorporate a watchdog timer reset in to the system of Reeves to increase fault handling abilities of Reeves, making a more robust system.

As per claim 17, Reeves does not explicitly disclose:

the ability for the host computer to reset the embedded processor.

Official Notice is given that it is notoriously well known for controllers to be reset by host systems in case of failure. Faults often occur that require a complete reset of devices. Host systems are well known to be it the unique of having control over some devices and having access to fault information and the ability to power cycles devices on some types of buses. Practitioners in the fault tolerant arts have been resetting controllers via hosts to improve the fault handling abilities and thus make the system able to withstand errors. Thus it would have been obvious to one of ordinary skill in the

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art incorporate controller reset via host computer into Reeves thus increasing the fault tolerance of the system of Reeves.

Claims 2-4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reeves (United States Patent No. 7,028,154 B2) in view of Wang (United States Patent No. 6,587,970).

As per claim 2, Reeves does not disclose but Wang teaches:

A method of using a controller of claim 1, the method comprising of the controller performing the following steps:

the controller determining or being told that the host computer has failed (column 2, lines 19-26);

transmitting NVRAM data to another computer (column 2, lines 19-26).

Wang provides a controller for handling the failover between two host system with access to a shared storage device. In fact, Wang meets structural and function limitations of claim 1 do not involve the power sourcing of the system. Reeves provides a controller for a similar storage system and describes in detail how the power and memory requirements are handled. Both system teach reliability enhancement through the well known concept of redundancy, either of controllers or servers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to

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incorporate the dual host system of Wang into the power protected controllers of Reeves thus creating fault hardened system.

As per claim 3, Reeves does not disclose but Wang teaches:

A method of using a controller of claim 1, the method comprising of the controller performing the following steps:

the controller determining or being told that the host computer has failed (column 2, lines 19-26);

responding to requests from another computer to transmit part or all of the NVRAM data (column 8, lines 4-14).

Wang provides a controller for handling the failover between two host system with access to a shared storage device. In fact, Wang meets structural and function limitations of claim 1 do not involve the power sourcing of the system. Reeves provides a controller for a similar storage system and describes in detail how the power and memory requirements are handled. Both system teach reliability enhancement through the well known concept of redundancy, either of controllers or servers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the dual host system of Wang into the power protected controllers of Reeves thus creating fault hardened system.

As per claim 4, Reeves does not disclose but Wang teaches:

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A duplicity of controllers of claim 1 connected to each member of a cluster of host computers and connected to each other by network interconnections, thereby enabling fail-over operations between cluster members (column 2, lines 50-55)

Wang provides a controller for handling the failover between two host system with access to a shared storage device. In fact, Wang meets structural and function limitations of claim 1 do not involve the power sourcing of the system. Reeves provides a controller for a similar storage system and describes in detail how the power and memory requirements are handled. Both system teach reliability enhancement through the well known concept of redundancy, either of controllers or servers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the dual host system of Wang into the power protected controllers of Reeves thus creating fault hardened system.

As per claim 4, Reeves does not disclose but Wang teaches:

A controller of claim 1 used as an NVRAM device that preserves data during long outages by sending it to another computer over a network such that the other computer can take over operations from the first host computer (column 7, lines 3-17).

Wang provides a controller for handling the failover between two host system with access to a shared storage device. In fact, Wang meets structural and function limitations of claim 1 do not involve the power sourcing of the system. Reeves provides

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a controller for a similar storage system and describes in detail how the power and memory requirements are handled. Both system teach reliability enhancement through the well known concept of redundancy, either of controllers or servers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the dual host system of Wang into the power protected controllers of Reeves thus creating fault hardened system.

Allowable Subject Matter

Claims 6 and 7 are objected while containing allowable subject matter. This subject matter, namely the processing of or message through the bridges, when claimed in conjunction with the remainder of the subject matter overcomes the prior art or record. Any modification to the claims may jeopardize this indication of allowable subject matter.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Bryce P Bonzo
Primary Examiner
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